Guest Editors' Introduction: Special Section on Computer Arithmetic

Peter Kornerup, Paolo Montuschi, Jean-Michel Muller, Eric Schwarz

Guest Editors' Introduction: Special Section on Computer Arithmetic

Peter Kornerup, *Member*, *IEEE*, Paolo Montuschi, *Senior Member*, *IEEE*, Jean-Michel Muller, *Senior Member*, *IEEE*, and Eric Schwarz, *Senior Member*, *IEEE*

COMPUTER arithmetic is the mother of all computer research and application topics, like *mathematics* (as the title of a famous book by E.T. Bell) is the *queen and servant of sciences* and *arithmetic the queen of mathematics*. The etymology itself of the word computer is intrinsically related to the concept of arithmetic and mathematics. Interesting to note is that the origin of the word computer comes from the Latin word computare, which is defined as count, evaluate, calculate the result. In all cases, the connection between computers and computer arithmetic goes beyond simple etymology reasons. Computers are designed either to perform a specific calculation or to have extensive programmability for many changing tasks. In either case, at a certain level this translates into doing computations and arithmetic evaluations. Just to give two examples:

- even for totally nonnumeric applications, processors keep on manipulating addresses of objects in memory, which requires additions, multiplications, and sometimes divisions;
- also, guaranteeing confidentiality and/or integrity of important data, as well as providing reliable electronic signatures, is done using cryptographic algorithms that make intensive use of arithmetic operations, either on integers or on elements of some finite fields.

Efficient computer arithmetic algorithms, fast implementations, robust designs utilizing appropriate and efficient number systems and representations, coupled with thorough verification, are all necessary issues for any fast computing and computer device. Speed is not the only one goal: High numeric precision, standardization of the results, low energy consumption, and fault-tolerant devices have become, in recent years, equally important issues which, in most cases, have to be explored in conjunction with the physical implementation technologies. For these reasons, computer arithmetic, besides the well-assessed results which have been obtained during the last decades, still remains a fertile and interesting area for research and innovation.

This special section hosts eight high quality research papers in computer arithmetic. They are the result of a selection from more than 60 submitted manuscripts in response to an open call for papers following the 17th and 18th IEEE International Symposium on Computer Arithmetic, which took place in Vail (Colorado) and Montpellier (France), respectively, in 2005 and 2007. All papers received peer reviews by expert referees and eight papers were selected for inclusion in this special section to represent a range of the topics of the papers having received all positive evaluations by the referees. Unfortunately, due to a limit on the number of papers that could be accommodated, some papers had to be postponed to later regular issues of these transactions. The papers in this special section are grouped into four categories: decimal arithmetic, number systems, multiplication and elementary functions, and formal proofs.

Decimal Arithmetic. The first paper is entitled "A Software Implementation of the IEEE 754R Decimal Floating-Point Arithmetic Using the Binary Encoding Format" and is authored by M. Cornea, J. Harrison, C. Anderson, P.T.P. Tang, E. Schneider, and E. Gvozdev. Decimal floating-point calculations are necessary for commercial financial transactions and this paper shows a new software implementation to this new standard. The standard provided two encodings of decimal format, a compressed BCD format and a binary encoded format. This paper shows how to overcome difficulties with a binary encoded coefficient. The paper provides some novel ideas on how to shift and round binary numbers to decimal radix points without using division.

Number Systems. Logarithmic number systems have been suggested as a way of representing real numbers. They allow for simple and fast multiplications and exponentiations, at the cost of significantly more complex additions and subtractions: whether they are interesting or not depends on the applications. The paper entitled "A Discrete Logarithm Number System for Integer Arithmetic Modulo 2^k: Algorithms and Lookup Structures", by A. Fit-Florea, L. Li, M.A. Thornton, and D.W. Matula, shows that these systems can also be adapted to integer arithmetic. Their system allows integer multiplication to be reduced to addition. They introduce several conversion algorithms.

Multiplication and Elementary Funtions. The paper "Low-Power Multiple-Precision Iterative Floating-Point Multiplier with SIMD Support" by D. Tan, C.E. Lemonds,

- *P. Kornerup is with the University of Southern Denmark, Odense, Denmark. E-mail: kornerup@imada.sdu.dk.*
- *P. Montuschi is with the Politecnico di Torino, Torino, Italy. E-mail: paolo.montuschi@polito.it.*
- *J.-M. Muller is with CNRS, Laboratoire LIP, INRIA Project Arénaire, Université de Lyon, France. E-mail: Jean-Michel.Muller@ens-lyon.fr.*
- *E. Schwarz is with IBM Corporation, 2455 South Road, Poughkeepsie, NY 12601. E-mail: eschwarz@us.ibm.com.*

For information on obtaining reprints of this article, please send e-mail to: tc@computer.org.

and M.J. Schulte presents the design of an IEEE-754 compliant floating-point unit that can perform two parallel single-precision multiplies every cycle with a latency of two cycles, or one double-precision multiply every two cycles with a latency of four cycles, or one extended-double-precision every three cycles with a latency of five cycles. Compared to previous designs with similar performance, it has 60 percent less area and 59 percent less dynamic power consumption.

The following paper, "Improved Computation of Square Roots in Specific Finite Fields" by D.-G. Han, D. Choi, and H. Kim, deals with efficient exponentiation such as for the special case of square root extraction in a finite field F_q, where q is a prime power.

The paper "An Efficient Rounding Boundary Test for $\mathrm{pow}(x, y)$ in Double Precision" is authored by C.Q. Lauter and V. Lefèvre. It discusses issues related to the very accurate implementation of the power function. If one wishes to guarantee correct rounding of that function (i.e., the returned result is always the floating-point number nearest to the exact value), one must be able to quickly detect when x^y is exactly halfway between two consecutive floating-point numbers. The authors suggest new tests for that purpose.

Saturated accumulation is an important operation in signal processing applications. The paper "Pipelining Saturated Accumulation" by K. Papadantonakis, N. Kapre, S. Chan, and A. DeHon shows how to reformulate saturated accumulation as an associative operation. This makes it possible to use a parallel-prefix scheme to perform saturated accumulation in a pipeline, at very fast data rates.

Formal Proofs. The paper "Kahan's Algorithm for a Correct Discriminant Computation at Last Formally Proven" by S. Boldo is the first of two papers on formal proofs. It gives a formal proof of an important and very accurate algorithm designed years ago by Professor William Kahan. Automating the formal proofs for this type of arithmetic algorithm is necessary because the pen-and-paper proofs are very long and tricky.

The second paper on formal proofs, authored by M. Daumas, D. Lester, and C. Muñoz, is "Verified Real Number Calculations: A Library for Interval Arithmetic." In this paper, the authors develop a rational interval arithmetic where real number calculations take place in an algebraic setting. This allows them to prove bounds on arithmetic expressions that contain elementary functions.

In conclusion, our special thanks go to the Editor-in-Chief, Professor Fabrizio Lombardi, for providing the opportunity to have a special section on Computer Arithmetic hosted by the *IEEE Transactions on Computers*. We thank all of the authors who submitted to this special section and the anonymous reviewers for their deep and constructive evaluations of the manuscripts. Our warmest thanks go to Joyce Arnold and Kathy Santa Maria for their professional and always helpful staff support.

Peter Kornerup
Paolo Montuschi
Jean-Michel Muller
Eric Schwarz
Guest Editors

Peter Kornerup received the Mag. Scient. degree in mathematics from Aarhus University, Denmark, in 1967. After a period with the University Computing Center, beginning in 1969, he was involved in establishing the computer science curriculum at Aarhus University, where he helped found the Computer Science Department in 1971 and where he served as its chairman until 1988, when he became a professor of computer science at Odense University, now the University of Southern Denmark. He spent a leave during 1975/1976 with the University of Southwestern Louisiana, Lafayette, four months in 1979 and shorter stays in many years with Southern Methodist University, Dallas, Texas, one month with the Université de Provence in Marseille in 1996, and two months with the École Normale Supérieure de Lyon in 2001 and further visits in the following years. Professor Kornerup has served on program committees for numerous IEEE, ACM, and other meetings; in particular, he has been on the program committees for the 4th through the 19th IEEE Symposium on Computer Arithmetic and served as program cochair for this symposium in 1983, 1991, 1999, and 2007. He has been a guest editor for a number of journal special issues, and served as an associate editor of the *IEEE Transactions on Computers* from 1991 to 1995. He is a member of the IEEE.

Paolo Montuschi graduated in electronic engineering in 1984 and received the PhD degree in computer engineering in 1989 from the Politecnico di Torino, Italy. Since 2000, he has been a full tenured professor with the Politecnico di Torino and, since 2003, he has been the chair of the Department of Computer Engineering at the Politecnico di Torino. Currently, he is involved in several management and directive committees at the Politecnico di Torino. From 1988 to 1994, he was a member of the Board of the Italian Association for Computer Graphics. From 1995 to 1997 and in 2006, he was deputy chair of the Center for Computing Facilities and Services of the Politecnico di Torino. Since 1997, he has been a member of the Steering Committee of the Post-Lauream Degree in Computer Networks and Multimedia Systems of Politecnico di Torino. He also worked as a visiting scientist with the University of California at Los Angeles and the Universitat Politecnica de Catalunya at Barcelona, Spain. Dr. Montuschi served on the program committees for the 13th through 19th IEEE Symposium on Computer Arithmetic and was program cochair of the 17th IEEE Symposium on Computer Arithmetic. From 2000 to 2004, he served as an associate editor of the *IEEE Transactions on Computers*. His current research interests cover several aspects of both computer arithmetic, with a special emphasis on algorithms and architectures for fast elementary function evaluations, and computer graphics. Dr. Montuschi is a member of the IEEE Computer Society and a senior member of the IEEE. Since 2006, he has been a member of the CPOC (Conference Publications Operations Committee) of the Computer Society. Since 2008, he has been a member-at-large of the Publication Board of the IEEE Computer Society.

Jean-Michel Muller received the PhD degree in 1985 from the Institut National Polytechnique de Grenoble. He is Directeur de Recherches (senior researcher) at CNRS, France, and he is the former head of the LIP laboratory (LIP is a joint laboratory of CNRS, the École Normale Supérieure de Lyon, INRIA, and the Université Claude Bernard Lyon 1). His research interests are in computer arithmetic. Dr. Muller was co-program chair of the 13th IEEE Symposium on Computer Arithmetic (Asilomar, June 1997), general chair of SCAN '97 (Lyon, France, September 1997), general chair of the 14th IEEE Symposium on Computer Arithmetic (Adelaide, Australia, April 1999). He is the author of several books, including *Elementary Functions, Algorithms and Implementation* (second edition, Birkhäuser Boston, 2006). He served as an associate editor of the *IEEE Transactions on Computers* from 1996 to 2000. He is a senior member of the IEEE.

Eric Schwarz graduated in 1983 from the Pennsylvania State University with the BSESc degree, in 1984 from Ohio University with the MSEE degree, and in 1993 from Stanford University with the PhD degree in electrical engineering. He joined IBM Corporation in 1984 and now works in Poughkeepsie, New York, where he is a Distinguished Engineer in the Systems and Technology Division. He has worked on the 9371, G4, G5, G6, z900, z990, z9 109, and z10 mainframe computers as well as the recent POWER6 processor. He was chief engineer on the z900 core introduced in 2000 and is currently the core architect on a future z Series core. He led the development of the first z Series FPU to implement IEEE 754 binary floating-point standard in 1998, the first z Series 64-bit processor, and the first hardware implementations of decimal floating-point units as specified in the new 754-2008 IEEE floating-point standard. Dr. Schwarz has 32 issued US patents and 33 filings pending. He is also the author of 20 journal articles and numerous conference papers. He has served on the program committees for the 13th through 19th IEEE Symposium on Computer Arithmetic and was program cochair of the 17th symposium in 2005. His research interests include computer arithmetic as well as computer architecture. He is a senior member of the IEEE.